REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

Claims 14-15 are pending before this amendment. No new matter has been added.

In the office action (page 2), claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 7,088,797 (Momtaz). The "et al." suffix is omitted in a reference name.

The applicant respectfully disagrees.

The present invention relates to a memory device for synchronization of an external input clock with an internal input clock that reduces power consumption when the device is in a power-down mode. The present invention prevents power waste by utilizing a clock divider that generates a clock signal having a frequency (for saving power) that is different from the frequency of the clock signal generated during the power up mode. For example, the power saving frequency of the clock signal generated during the power down mode would consume less electric current than the frequency generated during the power up mode of the memory device.

Thus, the presently claimed invention includes –a power down controller-- that determines a power down condition based on a clock enable signal and --the clock divider outputs a first clock signal being one of the output signals of the clock signal dividers excluding the last clock signal divider of the series when the synchronous memory device is in the power down condition--. The frequency of the fist clock signal is lower than that of the second clock signal in order to prevent power waste when the device is in a power-down mode.

In the office action (pages 2-3), the examiner points to the detector 202 of Momtaz as disclosing a power down controller and the cycle add/drop circuit 901/902 as disclosing the clock divider of the presently claimed invention. The applicant respectfully disagrees.

In Momtaz, the clock signal output of the phase locked loop indicates to the transmitter what the data rate of the data signal should be (Momtaz col. 3, lines 58-62). Thus, in Momtaz, the clock divider does not output a divided signal –when the synchronous memory device is in the power down mode– and instead, the device of Momtaz is operating normally (i.e., not powered down) when the cycle add/drop 901 and 902 are operating.

Further, in order to indicate to the transmitter what the data rate of the data signal should be, the cycle add/drop circuits simply drop one or more single clock cycles (see, e.g., Momtaz col. 5, lines 19-22 and FIG. 5, in which only a single clock cycle is dropped from RdCLK). This cannot be considered a power down mode in the present invention, in which the clock divider generates a clock signal having a frequency different (less) than the frequency during power up mode in order to conserve power, since Momtaz drops only a one or more single cycles (such as in FIG. 5) in order to indicate what the data rate should be.

For example, in Momtaz, the drop circuit 901 will remove a pulse width from RDclk or Vdclk so that PFD 202 will adjust the phase of signal Vdclk to match the phase of Rdclk. In this manner, Vcoclk can indicate to the transmitter what the data rate should be (see Momtaz col. 5 lines 65 to col. 6, line 13). Thus, this is not a power down mode and does prevent power waste, and is instead a method of indicated to the

transmitter what the transmitter's data transfer rate should be.

Accordingly, for at least this reason, the applicant respectfully submits that Momtaz does not teach or suggest the present invention of claim 14, which includes the power down controller for determining a power down condition, and the clock divider that outputs a first clock signal when the synchronous memory device is in the power down condition.

For the reasons set forth above, the applicant respectfully submit that claims 14-15 pending in this application are in condition for allowance over the cited references. Accordingly, the applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter.

This amendment is considered to be responsive to all points raised in the office action. Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

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